



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/757,866

01/16/2004

Craig Hansen

43876-156

5955

7590 11/05/2007
McDERMONTT, WILL & EMERY
600 13th Street, N.W.
Washington, DC 20005-3096

EXAMINER

COLEMAN, ERIC

ART UNIT

PAPER NUMBER

2183

MAIL DATE

DELIVERY MODE

11/05/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/757,866	Applicant(s) HANSEN ET AL.	
	Examiner Eric Coleman	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 August 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-18 and 28-41 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-18 and 28-41 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 35-41 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 35, (line 6) contains the language "data in at least one in a register file". It is unclear what "one" is referring to and therefore the scope of meaning of the claim is not clear. Claims 36-41 depend from claim 35 and therefore contain the same ambiguity.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1- 8,10-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hao (patent No. 4,569,016).
5. Hao taught the invention substantially as claimed including a data processing ("DP") system comprising (as to claim 1): A method for processing data using a programmable processor comprising: Decoding a single processor instruction for writing data to memory based on a mask and data contained in at least one register (e.g. see

Art Unit: 2183

figs. 2a,2b and col. 25,lines 23-66 and col. 26, lines 3-46), the mask comprising fields that each correspond to a field of the data contained in the at least one register(e.g., see col. 26,lines 36-46); detecting some of the fields of the mask as having a predetermined value to identify corresponding fields contained in the at least one register as write-enabled data fields(e.g., see col. 26, lines 26-46).

6. Hao did not expressly detail storing the result of a mask in memory. Hao taught storing the write enabled data fields to a specified register (e.g., see col. 13, lines 7-12) and taught the processor performs rotate operations on data from a general purpose register and returns the result, or portion of the result to a general purpose register or to main storage (e.g., see col. 12, lines 42-60). Therefore one of ordinary skill would have been motivated to store the result of the mask and rotate to main storage. The Hao system stores results in main storage and this would have reduced the number of registers needed to perform further processing.

7. As per claim 2, Hao taught each of the fields of the mask has a width of one bit (e.g., see col. 15, lines 39-44).

8. As per claim 3, Hao taught each of the fields of data contained in the at least one register has a width of one bit (e.g., see col. 15, lines 39-44).

9. As per claim 4, Hao taught the writing step further comprises reading an unaltered field of data from the specified memory location and writing the unaltered field of data along with the write-enabled data fields of the specified memory location (e.g., see col. 15, lines 39-44).

10. As per claim 5, Hao taught the mask is contained in a specified register (e.g., see col. 28, lines 21-54).

11. As per claim 6, Hao taught storing the result a memory location (e.g., see col. 12, lines 42-60). Therefore one of ordinary skill would have been motivated to provide the destination memory location in a register such as the instruction register when the destination address an immediate field or another register when the destination was specified using direct or indirect addressing.

12. As per claim 7, Hao taught the architecture comprising a 32-bit architecture (e.g., see col. 8, lines 64-68). Therefore one of ordinary skill would have been motivated to store the data or instructions to memory in specified memory locations comprises a section of memory having a specific width (e.g., 32-bits) and beginning at a specific memory address at least to allow later retrieval of stored data.

13. As per claim 8, Hao taught the predetermined logic value is 1(e.g. see col. 13, lines 6-15).

14. As per claim 10, Hao taught computer readable storage medium (main storage, and I-cache (e.g., see fig.1) stored therein a plurality of instructions that cause programmable processor to perform data operations: at least some of the instructions including a single instruction for selectively storing the single instruction capable of instructing the programmable processor to perform operations (e.g., see col. 12, line 56- col. 22, line 64) comprising: decoding the single instruction to obtain a mask and data contained in at least one register (e.g. see figs. 2a, 2b and col. 25, lines 23-66 and col. 26, lines 3-46), the mask comprising fields that each correspond to a field of the data

Art Unit: 2183

contained in the at least one register e.g., see col. 26, lines 36-46); detecting some of the fields of the mask as having a predetermined value to identify corresponding fields of the data contained in the at least one register as write-enabled data fields (e.g., see col. 26, lines 26-46). Hao did not expressly detail storing the result of a mask in memory. Hao taught storing the write enabled data fields to a specified register (e.g., see col. 13, lines 7-12) and taught the processor performs rotate operations on data from a general purpose register and returns the result, or portion of the result to a general purpose register or to main storage (e.g., see col. 12, lines 56-60). Therefore one of ordinary skill would have been motivated to store the result of the mask and rotate to main storage. The Hao system stores results in main storage and this would have reduced the number of registers needed to perform further processing.

15. As per claim 11, Hao taught each of the fields of the mask has a width of one bit(e.g., see col. 15, lines 39-44)..

16. As per claim 12, Hao taught each of the fields of the data contained in the at least one register has a width of one bit (e.g., see col. 15, lines 39-44).

17. As per claim 13, Hao taught the writing step comprises reading a unaltered field of data from the specified memory location and writing the unaltered field of data along with the write-enabled data fields to the specified memory location (e.g., see col. 15, lines 39-44).

18. As per claim 14, Hao taught the mask is contained in a specified register (e.g., see col. 28, lines 21-54).

19. As per claim 15, Hao taught storing the result a memory location (e.g., see col. 12, lines 42-60). Therefore one of ordinary skill would have been motivated to provide the destination memory location in a register such as the instruction register when the destination address an immediate field or another register when the destination was specified using direct or indirect addressing.

20. As per claim 16, Hao taught the architecture comprising a 32-bit architecture (e.g., see col. 8, lines 64-68). Therefore one of ordinary skill would have been motivated to store the data or instructions to memory in specified memory locations comprises a section of memory having a specific width (e.g., 32-bits) and beginning at a specific memory address at least to allow later retrieval of stored data.

21. As per claim 17, Hao taught the predetermined value is 1(e.g. see col. 13, lines 6-15).

22. Claims 9,18, are rejected under 35 U.S.C. 103(a) as being unpatentable over Hao applied to claims 1-8,10 above, and further in view of Kabir (patent No. 5,933,160).

23. As per claim 9, 18 Kabir taught decoding a second single instruction specifying a fourth register containing a plurality of floating point operands; multiplying the plurality of floating point operands in the third register by the plurality of operands in the fourth register to produce a plurality of products; and providing the partitioned field of a result as a concatenated result (e.g., see fig. 4, 5a, 5b and col. 8, lines 21-45).

24. It would have been obvious to one of ordinary skill to combine the teachings of Hao and Kabir. Both references were directed toward performing operations of partial

widths of data stored in registers. Kabir taught further operations to be performed on the partial width data such as multiplication on floating point data (e.g., see fig. 4) for performing image processing in a digital system (e.g., see col. 1, lines 6-11) consequently one of ordinary skill would have been motivated to incorporate the floating point operations to the Hao system at least to provide the capability use in addition applications such as graphics applications.

25. Claims 28-32 and 35-39 are rejected under 35 U.S.C. 102(b) as being anticipated by Hao et al. (patent No. 4,569,016).

26. As per claims 28, Hao taught a method for processing in a programmable processor the method comprising: Decoding a single instruction for performing a bitwise insert operation on data in at least one register in a register file within the programmable processor (e.g. see figs. 2a,2b and col. 25, lines 23-66 and col. 26, lines 3-46), the bitwise insert operation operating on a first operand and a second operand stored in the at least one register (e.g., see col. 26, lines 36-46); and for each bit in the first operand, the bitwise insert operation inserting the bit into a corresponding bit position in a destination value if a corresponding bit in the second operand has a first predetermined value (e.g., see col. 15, lines 39-44).

27. As per claim 29, Hao taught the first predetermined value is a logic 1 (e.g. see col. 13, lines 6-15).

28. As per claim 30, Hao taught for each bit in the first operand, a corresponding bit position in the destination value is maintained as unchanged if a corresponding bit in the second operand has a second predetermined value (e.g., see col. 15, lines 39-44).

29. As per claim 31, Hao taught the second predetermined value is 0 (e.g. see col. 13, lines 6-15).

30. As per claim 32, Hao taught storing the destination value result a memory location (e.g., see col. 12, lines 42-60).

31. As per claim 35, Hao taught A computer readable medium having stored therein a plurality of instructions that cause a programmable processor to perform operations on data stored in the programmable processor(e.g. see figs. 2a,2b and col. 25,lines 23-66 and col. 26, lines 3-46), the plurality of instructions comprising: an instruction that causes the processor to perform a bitwise insert operation on data in at least one register (e.g., see col. 26, lines 36-46) within the programmable processor, the bitwise insert operation operating on a first operand and a second operand stored in the at least one register in the register file; and wherein for each bit in the first operand, the bitwise insert operation inserts the bit into a corresponding bit position in a destination value if a corresponding bit in the second operand has a first predetermined value(e.g., see col. 15, lines 39-44).

32. As per claim 36, Hao taught the first predetermined value is 1(e.g. see col. 13, lines 6-15).

33. As per claim 37, Hao taught for each bit in the first operand, a corresponding bit position in the destination value is maintained as unchanged if a corresponding bit in the second operand has a second predetermined value (e.g., see col. 15, lines 39-44).

34. As per claim 38, Hao taught the predetermined logic value is 0(e.g. see col. 13, lines 6-15).

35. As per claim 39, Hao taught the destination value is stored into memory (e.g., see col. 12, lines 42-60).

36. Claims 33,34,40,41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hao as applied to claims 28,35 above, and further in view of Kabir.

37. As per claims 33,40 Kabir taught arithmetic operation where operands were stored in registers of 64-bit width (e.g., see col. 8, lines 5-37 and col. 9, line 27-col. 10, line 28 and fig.5A,5B). As to the operand being 64 bit width one of ordinary skill would have been motivated to use data with more bits such as 64, 128 etc to take advantage of the increasing capacity of industry standard memories, data paths and processors at the time of the claimed invention.

38. It would have been obvious to one of ordinary skill to combine the teachings of Hao and Kabir. Both references were directed toward performing operations of partial widths of data stored in registers. Kabir taught further operations to be performed on the partial width data such as multiplication on floating point data (e.g., see fig. 4) for performing image processing in a digital system (e.g., see col. 1, lines 6-11) consequently one of ordinary skill would have been motivated to incorporate the floating point operations to the Hao system at least to provide the capability use in addition applications such as graphics applications.

39. As per claim 34, Kabir taught executing a plurality of different group floating point operation that arithmetically operate on multiple floating point operands partitioned in fields of an operand register in the plurality of registers to produce a concatenated result that is returned to a register in the plurality of registers, wherein the concatenated result

Art Unit: 2183

comprises a plurality of individual floating point results (e.g., see fig. 4, 5a, 5b and col. 8, lines 21-45 and col. 5, lines 6-47 and col. 4, lines 23-64).

40. As per claim 41, Kabir taught instructions further comprises a plurality of different group floating-point arithmetic operations that arithmetically operate one multiple floating-point operands stored in partitioned fields of an operand register in the plurality of registers to produce a concatenated result that is returned to a register in the plurality of registers, wherein the concatenated result comprises a plurality of individual floating-point results (e.g., see col. 4, lines 23-61 and col. 7, line 7-col. 8, line 41).

Response to Arguments

Applicant's arguments with respect to claims 1-18, 28-41 have been considered but are moot in view of the new ground(s) of rejection.

Note: The applicant argues the priority for the instant application includes the '840 patent (and its appendix) and '599 patent (and its appendix) including bitwise masking. The Examiner however contends that the limitations of claims 9, 18, 33, 34, 40, 41, are not supported by the 840 or 599 patents).

The change scope of the amended claims has necessitated a new search.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

IBM technical disclosure (April 1,1990) article entitled Extended Rotate and Merge Instructions with Built-Masks disclosed instruction and system for rotating and masking data.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2183

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

EC

A handwritten signature in black ink, appearing to read 'Eric Coleman', with a stylized flourish at the end.

**ERIC COLEMAN
PRIMARY EXAMINER**